"Production Engineering Measure (PEM) in accordance with Step I of Signal Corps Industrial Preparedness Procurement Requirements No. 15, dated 1 Oct. 1958 for Gallium Arsenide Varactor Diode per Specification SCS-128, dated 2 March 1962 and Modification #1, 2 May 1962"

AD-405-775

THIRD QUARTERLY PROGRESS REPORT

December 1, 1962 - February 28, 1963

Submitted to:

Industrial Preparedness Activity
PEM and Facilities Procurement Branch
U. S. ARMY ELECTRONICS MATERIEL AGENCY
225 South Eighteenth Street
Philadelphia 3, Pennsylvania

Contract No. DA-36-039-SC-86736
Order No. 19058-PP-62-81-81

SYLVANIA SEMICONDUCTOR DIVISION
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ABSTRACT

Studies to obtain the processes necessary for the high volume production of gallium arsenide varactor diodes are described in this report. These investigations include diffusion, ohmic contacts, junction formation and packaging. A diffusion process utilizing zinc and arsenic as a diffusant source is described as well as a low resistance P-type contact and a successful procedure for a uniform mesa formation.

PURPOSE

The purpose of the work being carried out under this contract is to establish the producibility, in accordance with Steps I and II of Signal Corps Industrial Preparedness Procurement Requirements (SCIPPR) No. 15 dated 1 October 1958, of Gallium Arsenide Varactor Diode per Specification SCS-128, dated 2 March 1962. Fulfillment of the stated purpose is being accomplished by the completion of the major steps as follows:

1. Engineering work necessary to establish capability to manufacture the subject varactor diode on a pilot line basis. This includes the development of production processes, materials design, and test procedures suitable for fabrication of the diode in accordance with the requirements of specification SCS-128 (See Appendix A) on a volume basis.

2. Manufacture and submission of samples for evaluation and approval according to established schedules as follows:

   375 Engineering samples
   100 Preproduction samples

3. Design, development, procurement and/or fabrication of production type equipment necessary to manufacture and test units meeting the above mentioned specification at the rate of 200 per day on a single eight (8) hour shift basis.

4. A production type run of 1000 units for the purpose of demonstrating the capability of the pilot line processes and equipment to manufacture at the specified rate of 200 units per eight (8) hour day in accordance with the applicable device specifications.

5. Submission of monthly, quarterly, and final reports.

6. Preparation of a report in accordance with Step II of SCIPPR No. 15 outlining steps required to establish production of units meeting the applicable specification at the rate of 2000 units per eight (8) hour day.

1.0 Narrative and Data

1.1 DIFFUSION

Wafers are prepared for diffusion by etching them in an HF + HNO_3 solution to reduce the thickness of the slice to 0.011 inches. A final etch of H_2O_2 + H_2SO_4 is used to polish the $(\bar{1}\bar{1}\bar{1})$ face and to decrease the thickness to the desired 0.010 inches. This preparation procedure minimizes the surface damage and thus allows for shallower diffusions. In addition use of the H_2SO_4 + H_2O_2 solution makes it possible to identify the $(\bar{1}\bar{1}\bar{1})$ face easily. This is necessary, since it has been found that etching is more uniform on this face and therefore, is the side used for mesa formation.

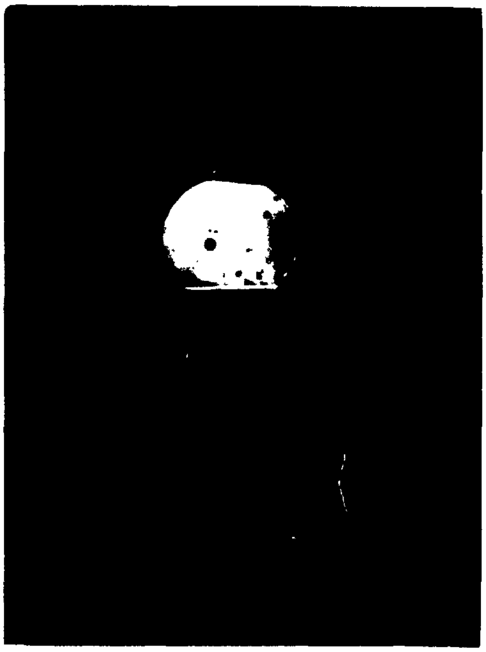
After diffusing with a Zn or Zn + Ga source according to the procedure described in the second quarterly report, a rough hazy surface (Figure 1) results on both sides of the wafer. At first it was thought that this condition was caused by the diffusant condensing on the wafer during the cooling cycle. This idea was disproved by quenching one end of the tube which condensed the vaporized diffusant in the cooled end. Although this procedure cleaned up the wafer somewhat, the surface of the wafer was still visibly disturbed. It was concluded that the surface problem was caused by a loss of arsenic during diffusion.

To overcome this loss, an arsenic vapor pressure was put in the tube during an elemental zinc diffusion by loading in 99.99% pure As. The diffused wafer came out perfectly smooth as illustrated in Figure 1. The additon of an arsenic pressure was tried also during a Zn-Ga diffusion, but with poor results. The arsenic reacted with the gallium to grow gallium arsenide from dilute solution. Consequently, the diffusions done during the latter part of this period have utilized elemental zinc with an arsenic background pressure. In addition, in order to keep the tube and wafer as clean as possible, one end of the ampoule is cooled immediately after withdrawal from the diffusion furnace.

The capacitance versus voltage variation in the above type diffusion is different than in previous diffusions. The n = .44 in the relationship:

$$C_J = \frac{Co}{\left(1 - \frac{V_{app}}{\phi}\right) n}$$

using zinc and arsenic as a source. The (n) in the diffusions described in preceding reports was .33 and .5 (see Figure 2).

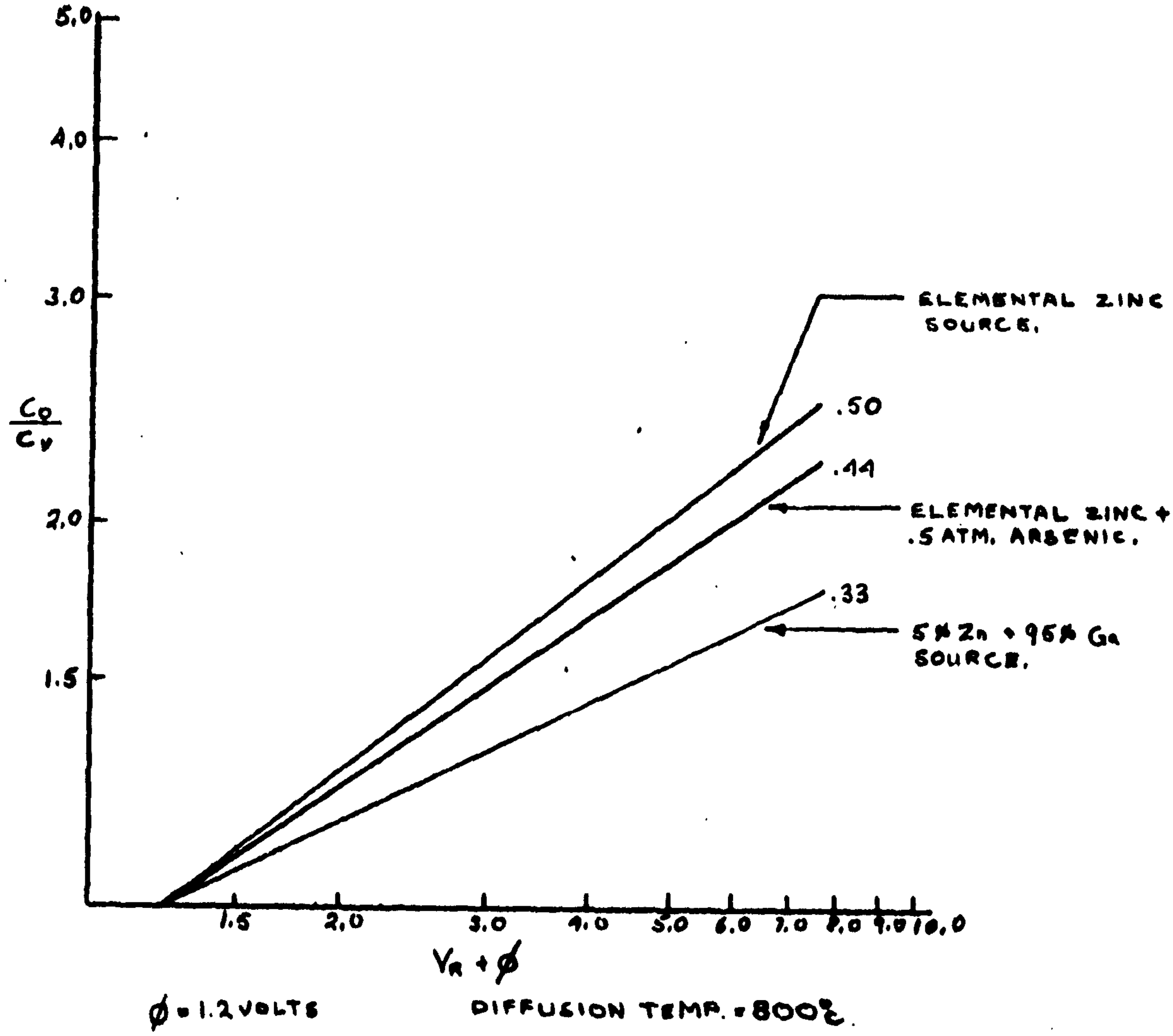


Hazy Surface
(No As pressure)

Smooth Surface
(.5 atm As pressure)

FIGURE 1

Ga As SURFACES WITH AND WITHOUT ARSENIC PRESSURE DURING DIFFUSION



CAPACITANCE VERSUS VOLTAGE DEPENDENCE FOR ELEMENTAL ZINC, ZINC-ARSENIC AND ZINC - GALLIUM DIFFUSION SOURCE

Figure 2

1.2 OHMIC CONTACTS

A significant increase in the adherence and lowering of the resistance of the P-type contact was attained during the past quarter. By changing the processing and increasing the amount of contact material, an improved and reproducible alloy was obtained. The series resistance of the diodes was lowered sufficiently to make possible the fabrication of several diodes with cutoff frequencies in excess of 200 Kmc at -6 volt bias. These results were repeated on several wafers to substantiate reproducibility. Prior to evaporation of the P-type contact the wafers are etched in HF for approximately five minutes and after rinsing are dried in instrument air. A Au-Zn alloy is evaporated through a .002 inch diameter mask. The mask is carefully removed so as not to smudge the evaporated dots; to prevent smearing the dots, a jig was built to insure removing the mask and holder in a vertical direction. Alloying of these dots is accomplished immediately after removing the wafer from the evaporator in order tc minimize exposure to the air.

The slice, coated with P-type contacts, is given a thirty second preheat at 250°C before being pushed into the 500°C zone of the furnace for three minutes. The gas flowing through the furnace is hydrogen which as a reducing atmosphere facilitates a smooth alloy to the surface of the gallium arsenide.

1.3 MESA FORMATION

After much investigation it was found that Kodak Photo Resist (KPR) did not adhere well enough on the small mesa areas to mask them against intensive etching. The KPR peeled off repeatedly after a specific length of etching time.

Kodak Metal Etch Resist (KMER) was investigated and is being used successfully in place of the KPR. The KMER is extremely resistant to etching and is as easy to apply as the former. The KMER is flowed onto the P-type side of the wafer which has 0.002" alloyed dots spaced at 0.020" intervals. The wafer is rotated at a constant RPM for one minute in order to insure a uniform layer thickness. The excess KMER is thrown off by the centrifugal force of the rotation. A one-hour bake at 65°C is sufficient to harden the KMER enough for further processing.

Photographic masks have been developed in order to make possible the use of photo resist techniques. The facilities and techniques of the Sylvania Advanced Development Group were utilized to develop these masks. The fabrication of these masks is quite a difficult and elaborate process due to the fact that an 0.002" diameter dot must be repeated sixty times at 0.020" intervals in all directions to product a 1 1/4" X 1 1/4" array. Any minute error in spacing will be magnified across the array and result in a faulty mask. Consequently, tolerances on these masks must be kept to less than 0.0001". A negative mask with 0.006" holes on 0.020" X 0.020" centers is illustrated in Figure 3.

The procedure in developing a precise 0.0015" or 0.002" mask consists of drawing a perfect master dot several thousand times larger than the required size. This dot is photographed and reduced in size with a system of lenses until it is the desired size of 0.0015" or 0.002" diameter.

The reduced dot is photographed and put into a step and repeat machine which accurately places and exposes these dots on film at 0.020" intervals.

An entire array 1 1/4" x 1 1/4" consists of almost 4000 precision dots. Photographic negatives (Figure 3) of positive plates can be made from the master film. After hardening the KMER, the wafer is placed in a jig previously developed by the transistor group at Sylvania's expense. This jig holds the slice by vacuum and permits the mask to be moved above it (Figure 4). When alignment is attained, as seen through the microscope, vacuum #2 is turned on to hold the plate in position. The vacuum chuck is then exposed under a mercury arc lamp following which the slice is placed into a developer solution. The unexposed areas are removed by the developer leaving the exposed mesa areas covered with KMER. The masked slice is then baked to further harden the KMER coating and make it more resistant to etching.

After baking, the wafer is etched in a 25^0C 18 HF + 1 HNO_3 solution until by probing it is found that the diffused P layer has been removed between the mesas. The time for this operation varies with the diffusion depth.

The KMER is removed from the top of the mesas by agitating a sufficient length of time in triad. The resultant 0.002" diameter mesa is illustrated in Figure 6 where it has been magnified 225 X.

A final HF + HNO_3 etch is given to the individual diodes after mounting in the package and thermal compression bonding in order to bring the junction capacitance down to the desired value. In the past a problem was encountered in this etching procedure. The time for etching the individual mesas varied extremely from diode to diode; this could have been caused by poor wetting of the acid around the junction. By ultrasonically cavitating the solution during the etch, this problem has been eliminated, and uniform capacitance values are obtainable within a given etching time period. Generally a five second etch is sufficient to bring the capacitance into the desired range.

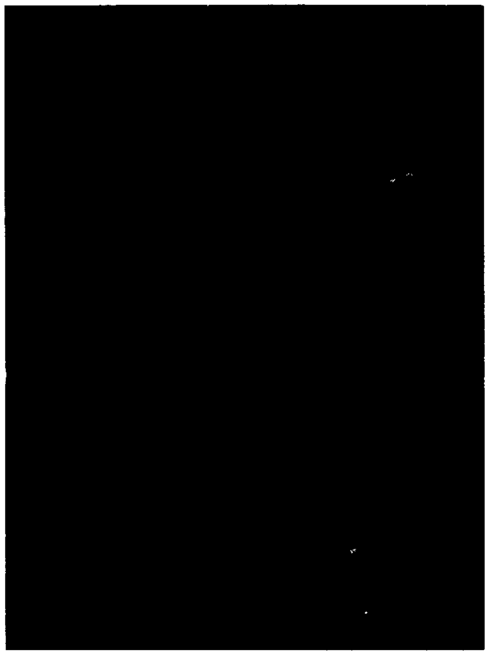
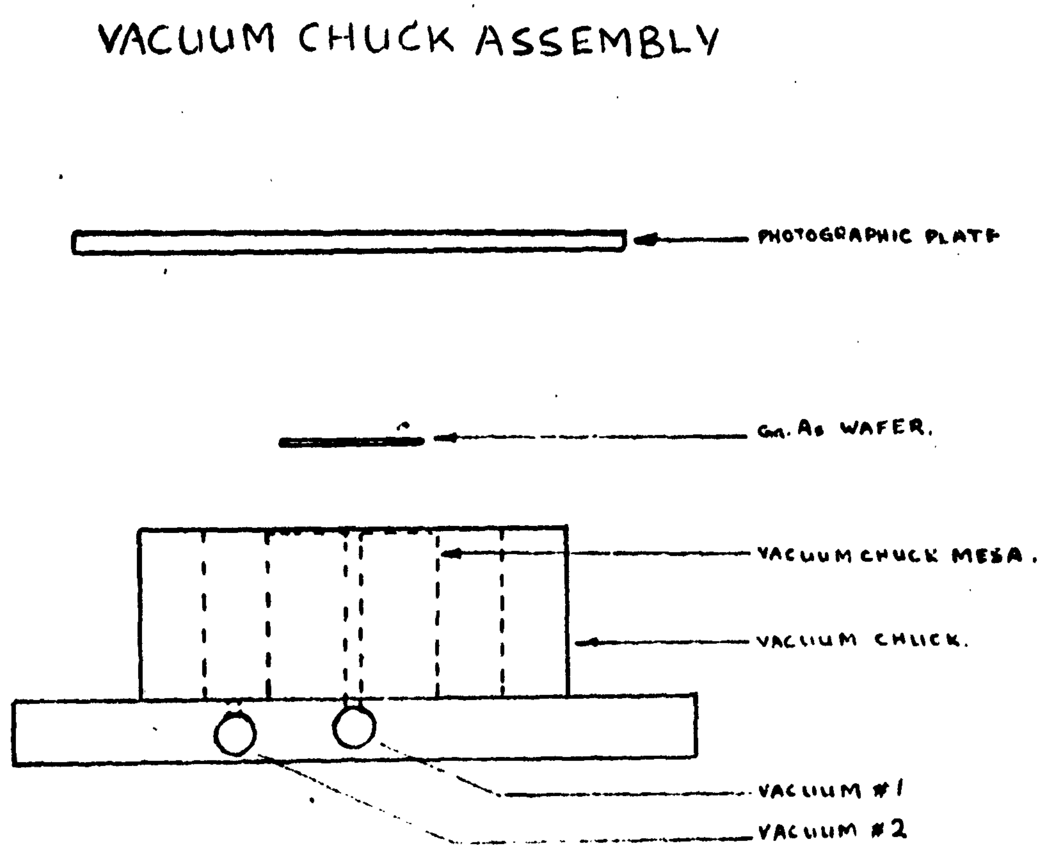


FIGURE 3

MASK USED IN KMER MESA FORMATION


VACUUM CHUCK ASSEMBLY
PHOTOGRAPHIC PLATE
Ga. As WAFER.
VACUUM CHUCK MESA.
VACUUM CHUCK.
VACUUM #1
VACUUM #2

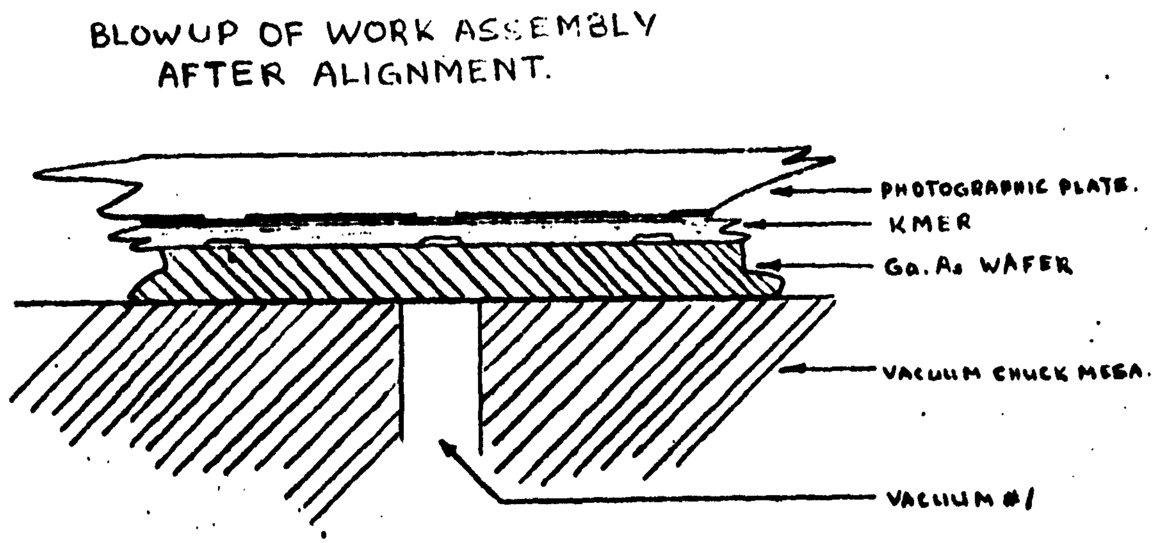

BLOWUP OF WORK ASSEMBLY
AFTER ALIGNMENT.
PHOTOGRAPHIC PLATE.
KMER
Ga. As WAFER
VACUUM CHUCK MESA.
VACUUM #1

Figure 4

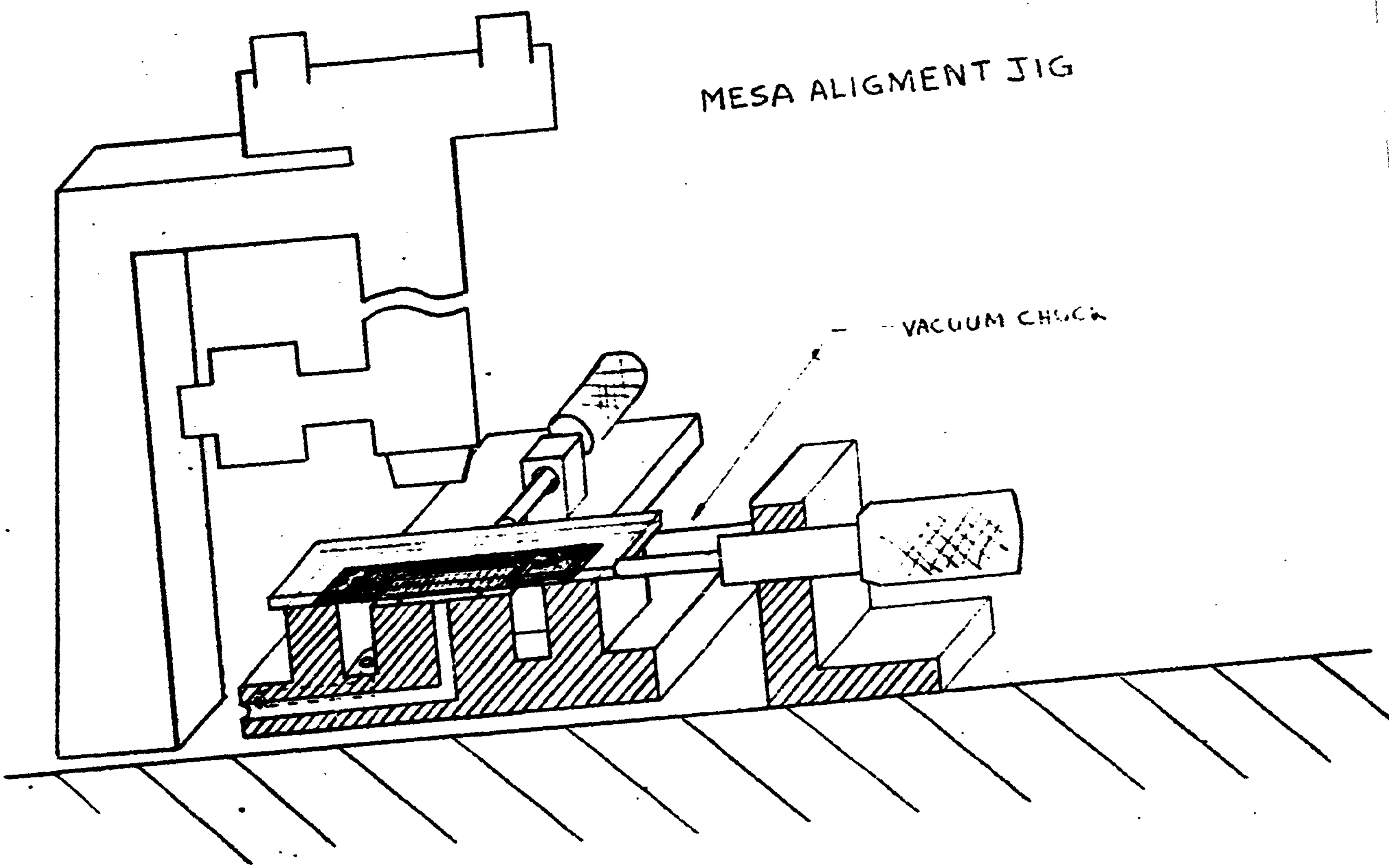


Figure 5

FIGURE 6

2 MIL MESA FABRICATED BY KMER TECHNIQUE (225 X)

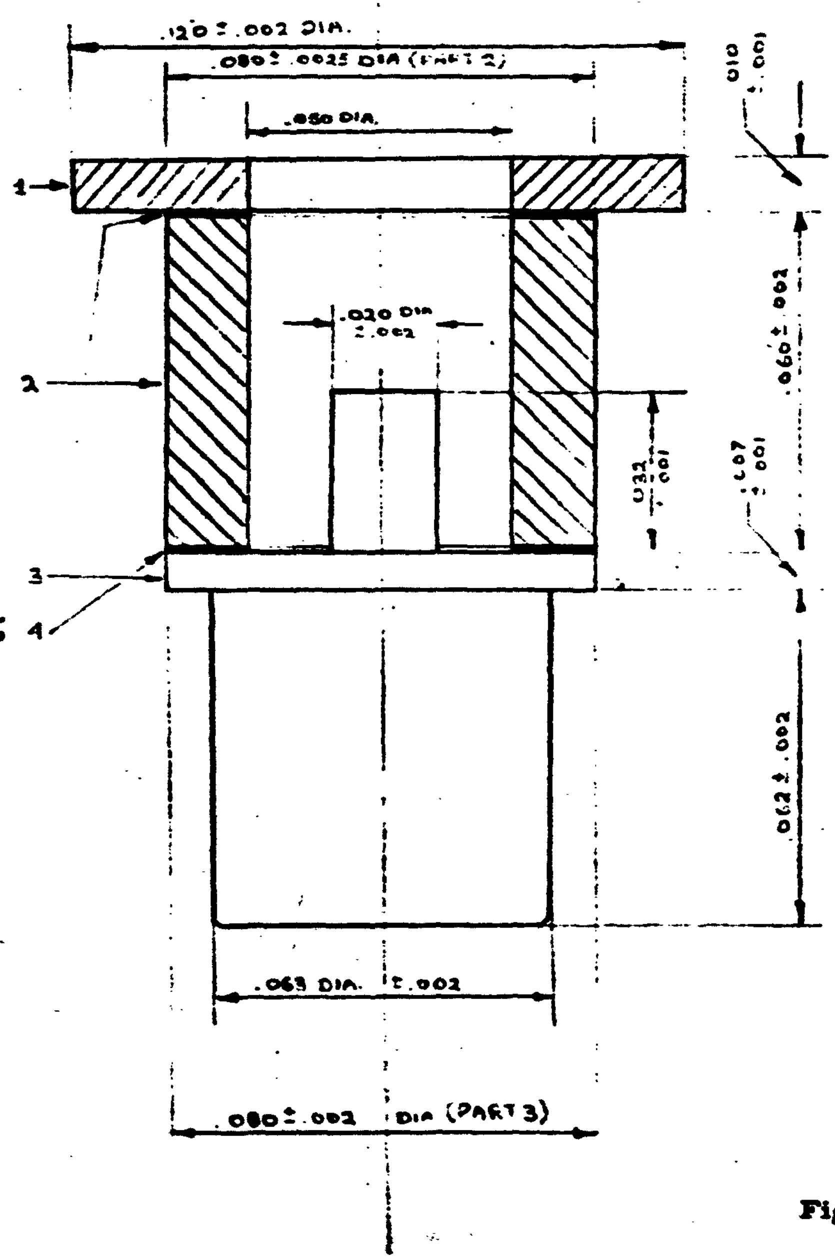
1.4 PACKAGING

Thirty prototype packages were received from Ceramics International as per Figure 7. The capacitance of this configuration is .146 uuf which meets the contract specifications (see Appendix A). The ceramic is fabricated of alumina with a wall thickness of 0.015". The wall thickness is limited by strength considerations since it is most desirable to have it as thin as possible for minimum capacitance. Diodes have been fabricated in these packages and some of them will be included in the next 75 engineering samples.

The second group of engineering samples which were delivered on January 30, 1963 were packaged in two different configurations. One package had a capacitance of 0.35 uuf (Figure 8) and the other had a capacitance of .22 uuf (Figure 9). An 0.7 mil gold wire was thermal compression bonded from the mesa to the flange in both configurations. The series inductance of the two latter assembled packages was measured at 1 Kmc in a 50 ohm line using a conductor with the same external dimensions as the packages measured for a reference point. The package in Figure 9 with a Cp = 0.22 uuf has a series inductance (Ls) = 0.9 nh while the shorter package in Figure 8 with a Cp of 0.35 uuf has an Ls = .7 nh. The high values of inductance can be attributed to the thin contact wire in these packages used for ease of fabrication. Steps are being initiated to fabricate diodes with a ribbon-type contact in order to decrease the series inductance.

Since there are problems involved in contacting a wide ribbon to a small mesa, a fine gold mesh has been designed which will also be tried in order to compare its inductance with that of an equal sized ribbon.

PROPOSED GA AS VARACTOR PACKAGE ASSEMBLY



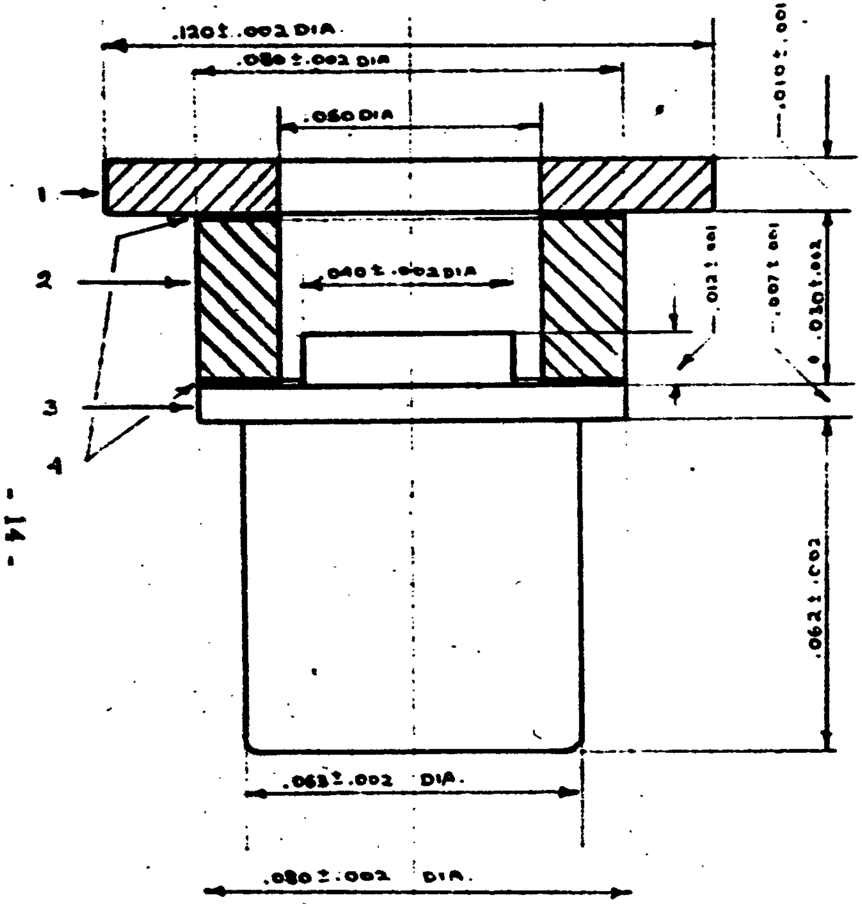
PART	QUANT	DESCRIPTION	MATERIAL
1	1	WASHER	KOVAR OR EQL
2	1	SHELL	75% AL_2O_3
3	1	PIN CAP	KOVAR OR EQL
4	2	PRE FORM	
		FOR 1-2 & 2-3	B.T. V.T G

NOTES:

1. SHADED AREAS DENOTE METALLIZING
2. ASSY MUST WITHSTAND 10 LBS PULL TEST.
3. ASSY MUST WITHSTAND 10 LBS SHEAR TEST.
4. .120 D & .062 D MUST BE CONCENTRIC WITHIN .002 T.I.R.

Figure 7

FIRST GA AS VARACTOR PACKAGE ASSEMBLY



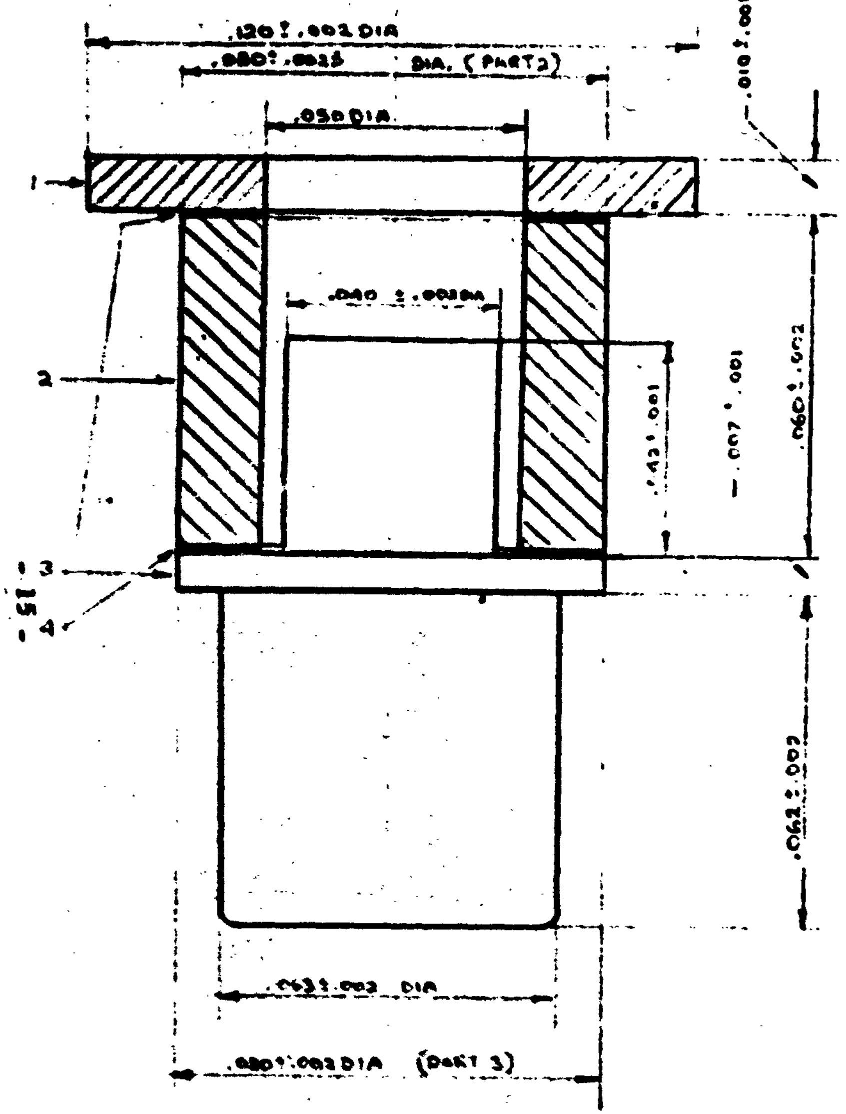
PART	QUANT.	DESCRIPTION	MATERIAL
1	1	WASHER	KOVAR OR EQL.
2	1	SHELL	95% Al_2O_3
3	1	PIN CAP	KOVAR OR EQL.
4	2	PRE FORM FOR 1-2 & 2-3	B.T. V.T.G

NOTES:

1. SHADED AREAS DENOTE METALLIZING.
2. ASS'Y MUST WITHSTAND 10 LBS. PULL TEST
3. ASS'Y MUST WITHSTAND 10 LBS. SHEAR TEST.
4. .120 DIA. & .063 DIA. MUST BE CONCENTRIC WITHIN .004 T.I.R

Figure 8

SECOND GA AS VARACTOR PACKAGE ASSEMBLY



PART	QUANT.	DESCRIPTION	MATERIAL
1	1	WASHER	KOVAR OR EQL.
2	1	SHELL	95% Al_2O_3
3	1	PIN CAP	KOVAR OR EQL.
4	2	PREFORM	
		FOR 1-2 & 2-3	B.T. V.T.G

NOTES:

1. SHADED AREAS DENOTE METALLIZING
2. ASS'Y MUST WITHSTAND 10 LBS. PULL TEST.
3. ASS'Y MUST WITHSTAND 10 LBS. SHEAR TEST.
4. .120 DIA & .063 DIA. MUST BE CONCENTRIC WITHIN .004 T.I.R.

- Figure 9

1.5 ENGINEERING SAMPLES

Seventy-five engineering samples were delivered to the U. S. Army Electronic Research and Development Laboratory in Fort Monmouth, New Jersey according to schedule on January 30, 1963. These diodes were vacuum baked at 200°C for thirty minutes prior to the final sealing which was carried out in a controlled environment with a dew point of -90°F. The samples (see Appendix B) showed a significant improvement in comparison to the first lot of 75 units delivered to the Signal Corps on November 30, 1962. The average frequency cutoff improved by almost 30 percent from an average of 66 Kmc to 85 Kmc. The junction capacity spread on the second set of samples, for the most part, was within the desired SCS-128 specification (see Appendix A). The junction capacitance of the first set of units ranged between 0.025 uuf and 2.45 uuf while the second lot ran between 0.087 and 1.28 uuf.

The wafer used for this pilot run was from an ingot horizontally grown by Monsanto Chemical Company and oriented on the $[111]$ axis. The resistivity of the slice was .0037 ohm-cm and had a Hall mobility of 2700 cm^2/volt sec.

The slice was etched in a $H_2SO_4 + H_2O_2$ solution which polished and thus distinguished the $(\bar{1}\bar{1}\bar{1})$ face. The wafer was diffused at 800°C with an elemental zinc source. The penetration depth on the As side was approximately .2 mils. The N-type contact was put on the Ga face and consisted of Au-Sn which was evaporated and alloyed in forming gas. The P-type contact was evaporated through a 1 x 2 mil mask and was sintered at 500°C in forming gas.

The mesas were masked by wax evaporation and etched until the desired capacitance value was reached. The dice were header mounted with Au-Sb

preforms and an 0.7 mil Au wire was attached to the mesa by thermal compression bonding. Before final sealing, the individual diodes were given a final etch when necessary to bring the capacitance into the specified by SCS-128.

2.0 Conclusions

During the past quarter, the second group of 75 engineering sample diodes were manufactured and sent to the United States Army Electronic Research and Development Laboratories for evaluation.

Investigations have continued in order to evolve the procedures necessary for the high volume production of gallium arsenide varactors.

A P-type production contact has been developed which has a sufficiently low resistance to make possible the production of varactor diodes with frequency cutoffs in excess of 200 Kmc.

3.0 PROGRAM FOR NEXT INTERVAL

1. Fabricate two groups of seventy-five engineering samples for delivery on March 31, 1963 and May 31, 1963.

2. Investigate foil and ribbon type contact in order to lower the inductance of the present package.

3. Continue refinement and simplification of processes in order to facilitate volume production.

Note: A planning and scheduling chart breaking down the major tasks into five divisions is shown in Figure 10.

Figure 10

SEMICONDUCTOR DIVISION, SYLVANIA ELECTRIC PRODUCTS INC.
PROJECT PERFORMANCE AND PLANNING SCHEDULE

Contract No. DA-36-039-SC-86736
Order No. 19058-PP-62-81-81

% Completion Information
as of February 28, 1963

Schedule: 1962 (J J A S O N D) — 1963 (J F M A M J J A S O N D) — 1964 (J F M A M J)

1-1	**Engr.-Prod. Device Processes**	
	Diffusion	
	a. Furnace Set Up & Calibration	COMPLETED
	b. Const. of Diff. Prep. Equip.	COMPLETED
	c. Diff. Parameters (prel. sel.)	COMPLETED
	d. Diff. Parameters (final sel.)	75%
	e. Final Prod. Type Diff. Proc.	
	Contacting	
	N-Type	
	a. Prel. Dec. Prod. Type Cont.	COMPLETED
	b. Sel. Final Contact	80%
	c. Final Prod. Cont. Process	
	P-Type	
	a. Prel. Dec. Prod. Type Cont.	COMPLETED
	b. Selection Final Contact	75%
	c. Final Prod. Contact Proc.	
	Packaging	
	a. Prel. Study of Parameters	80%
	b. Decision Best Combination	80%
	c. Finalized Package Design	75%
	Sealing Package	
	a. Init. Welder SetUp Contr. At.	COMPLETED
	b. Prel. Sealing Processes	COMPLETED
	c. Finalized Sealing Processes	90%
	Measurements	
	a. Reflectometer Set Up	COMPLETED
	b. Capacitance Measurement Set Up	COMPLETED
	c. Contract Holder Set Up	COMPLETED
	d. Compl. Prod. Meas. Opera.	
1-1-1	75 Engineering Samples	COMPLETED
	75 Engineering Samples	COMPLETED
	75 Engineering Samples	X
	75 Engineering Samples	X
	75 Engineering Samples	X
1-1-2	100 Preproduction Samples	
1-2	Production Type Equip	40%
1-3	1000 Pilot Prod. Units	X

Figure 10

SEMICONDUCTOR DIVISION, SYLVANIA ELECTRIC PRODUCTS INC.
PROJECT PERFORMANCE AND PLANNING SCHEDULE

		1962							1963													1964					
		J	J	A	S	O	N	D	J	F	M	A	M	J	J	A	S	O	N	D	J	F	M	A	M	J
1-4	Reports																									
1-4-1	Monthly																									
1-4-2	1st Quarterly Report (draft) Distribution	COMPLETED																								
	2nd Quarterly Report (draft) Distribution	COMPLETED																								
	3rd Quarterly Report (draft) Distribution	COMPLETED																								
	4th Quarterly Report (draft)														X											
	Distribution															X										
	5th Quarterly Report (draft)																	X								
	Distribution																		X							
	6th Quarterly Report(draft)																				X					
	Distribution																					X				
	7th Quarterly Report (draft)																							X		
	Distribution																								X	
1-4-3	Final Report - Step I (draft)																								X	
	Distribution																									X
1-4-4	Bills of Material & Parts																								X	
2	General Report-Step II(draft)																								X	
	Distribution																									X

4.0 MAN HOURS OF WORK PERFORMED

Engineers	Third Quarter	9 Month Cumulative Total
T. Baker	432	1224
G. Bowne	36	153
G. Ching	13	99
F. Tausch	32	232
H. Ramsey	-	15
K. Gunn	32	32
Technicians		
W. Hyde	-	18
E. Juleff	88	496
D. Johnson	-	324
E. Penny	-	116
A. Marmiani	424	1056
G. Kokk	488	872
F. Skalkos	68	140
R. Greene	-	1.5
D. Hapgood	40	40
Operators		
Grade 5 Operators	49	130
TOTAL HOURS	1702	4948.5

5.0 VISITS

December 20, 1962 - Mr. S. Sokolove, USAEMA, visited Woburn to review contract progress. A review was made of each of the processes and the new KPR process was demonstrated. The new package design was described and a thorough analysis made of the data. The problems involved in recuding contact resistance to the mesa were discussed and the solutions for the same which involve double diffusion and different contact materials.

January 28, 1963 - Mr. G. Hall, USAERDA, visited Woburn, and discussions were held regarding the contract progress with special regard to the correlation of USAERD diode holders to Sylvania.

APPENDIX A

Signal Corps Technical Requirements
SCS-128, 2 March 1962

(and Amendment #1, 2 May 1962 See Note #9)

SIGNAL CORPS
TECHNICAL
REQUIREMENTS

SCS-123
2 March 1962

SEMICONDUCTOR DIODE, GALLIUM ARSENIDE, VARACTOR, MICROWAVE TYPE SigC-IN(X-2)

1. SCOPE

1.1 Scope.- This document covers the detail requirements for gallium arsenide, variable reactance, semiconductor diodes for application as low-noise amplifiers in microwave-frequency receiver circuits, and capable of proper performance (see 3.4 herein) under the following conditions. (See 3.2 herein):

	Operating temperature	Operating altitude	Operating CW dissipation	Reverse voltage
	°C	ft.	mW	Vdc
Minimum	---	---	500	6.0
Maximum	200	Any	---	---

2. APPLICABLE DOCUMENTS

2.1 The following documents, of the issue in effect on date of invitation for bids, form a part of this specification to the extent specified herein:

SPECIFICATIONS

MILITARY

MIL-S-19500 Semiconductor Devices, General Specification For

STANDARDS

MILITARY

MIL-STD-15 Electrical and Electronic Symbols
MIL-STD-202 Test Methods for Electronic and Electrical Component Parts

SCS-128

DRAWINGS

SIGNAL CORPS

SC-A-46600 Preproduction Sample Approval In Lieu Of Qualification Requirements In Specifications

(Copies of specifications, standards, drawings, and publications required by contractors in connection with specific procurement functions should be obtained from the procuring agency or as directed by the contracting officer. Both the title and number or symbol should be stipulated when requesting copies.)

3. REQUIREMENTS

3.1 Requirements.- Requirements for the semiconductor diodes shall be in accordance with Specification MIL-S-19500, and as specified herein.

3.2 Abbreviations and symbols.- The abbreviations and symbols used herein are defined in Specification MIL-S-19500, and as identified in Tables I and II, and paragraphs 4.8.1 through 4.8.8 herein.

3.3 Design and construction.- The design and construction of the semiconductor diodes shall be in accordance with requirements of Specification MIL-S-19500, and shall be compatible with intended installation and application of the devices.

3.3.1 Operating position.- The semiconductor diodes shall be capable of proper operation in any position.

3.3.2 Polarity indication.- The graphic symbol for polarity indication on the semiconductor diodes shall be as designated in Standard MIL-STD-15.

3.4 Performance characteristics.- The semiconductor diode performance characteristics shall be as specified in Tables I and II herein. (See 6.3 herein.)

3.5 Marking.- The semiconductor diodes shall be marked in accordance with Specification MIL-S-19500 and as follows. In instances where the diminutive size or lack of suitable surface area on the device would prevent a marking accomplishment readable by the unaided eye, 20/20 vision, at eight inches distance from the device, such marking may be omitted directly on the device. All required marking shall be placed on the unit package.

3.5.1 Type-designation marking.- The semiconductor diodes shall be marked with the letters "SigC" and the "1N" designation of the device. The "1N" designation of the device shall be "(X-2)" until an identification number conforming to type designation requirements of Specification MIL-S-19500 has been established.

4. QUALITY ASSURANCE PROVISIONS

4.1 General.- Except as otherwise specified herein, the responsibility for inspection, general procedures for acceptance, classification of inspection, and inspection conditions and methods of test shall be in accordance with Specification MIL-S-19500, Quality Assurance Provisions.

4.2 Preproduction Sample Approval.- The Preproduction Sample Approval requirements in Signal Corps Drawing SC-A-46603 hereby replace any Qualification requirements referable to the product covered herein.

4.3 Sampling and acceptance criteria for Acceptance Inspection (see 6.2 herein).- For all tests except Life tests, sampling and acceptance criteria shall be in accordance with paragraphs 4.3.1 and 4.3.2, respectively, herein. For Life tests, sampling and acceptance criteria shall be in accordance with requirements for Method B in Specification MIL-S-19500, Appendix C. The respective LTPD (Lot Tolerance Percent Defective) and Max. Acc. No. (Maximum Acceptance Number) requirements in Tables I and II herein shall govern relative to the details in paragraphs 4.3.1 and 4.3.2 herein.

4.3.1 Sample size.- The sample size shall be selected by the manufacturer, using Table III herein. The sample size so chosen shall be within the Max. Acc. No. limit associated with the LTPD specified in Tables I and II herein.

4.3.2 Sample acceptance criteria.- For the sample size tested, the Acceptance Number "(a)" in Table III shall not be exceeded. (Rejection Number "r" = "(a)" +1).

4.3.3 Tightened inspection.- Tightened inspection on resubmitted lots is obtained by testing to an LTPD equal to or less than one-half of the specified initial LTPD.

4.4 Specified LTPD and Max. Acc. No.- The LTPD and Max. Acc. No. specified for a subgroup in Tables I and II herein shall apply for all of the tests, combined, in the subgroup.

4.5 Destructive tests.- None.

4.6 Disposition of sample units.- Sample units that have been subjected to and have passed Group B, Subgroups 2, 3, 4, and 5 tests may be delivered on the contract or order provided that, after Group B inspection is terminated, those sample units are subjected to and pass Group A inspection. Defective sample units from any sample group that may have passed group-inspection acceptance criteria shall not be delivered on the contract or order until the defect(s) has been remedied to the satisfaction of the Government.

4.7 Holder for test measurements.- The semiconductor diode shall be affixed within the holder specified in Figure 1 herein for all electrical test measurements.

4.8 Particular examination and test procedures.-

4.8.1 Frequency Cutoff test.- This test may be performed in accordance with Method A or Method B, following:

(a) Method A: Applying the condition specified for the test (see Table I herein), the test shall be performed using a test circuit mutually agreed upon between the contractor and th authorized Government technical representative. The cutoff frequency determination shall be based on the measurement of the 10 kmc or higher small-signal reflection coefficient of the tunable holder containing the diode. The applied microwave signal level shall be such that a 6 db increase in level does not change the measured cutoff frequency by more than 10%.

(b) Method B: The frequency cutoff may be computed from the formula: $f_c = Q \times$ frequency of measurement (10 kmc or higher), where Q is determined from the test procedure for the Diode Q test (see Table I herein). The condition specified for f_c (See Table I herein) shall be applicable.

4.8.2 Diode Q test.- The diode Q may be determined in accordance with computations per (a) or (b) below. Test circuitry shall be as mutually agreed upon between the contractor and the Contracting Officer's technical representative. It should be noted that the presentations in (a) and (b) below are based upon Smith Chart plot of the diode impedance as a function of frequency. The impedance of the diode as a function of frequency will rotate along a constant resistance circle, and the self-resonance frequency will coincide with the point of minimum VSWR and the crossing of the real axis on the Smith Chart.

(a) The diode Q (including the effect of strays) at resonance may be computed from the following:

$$Q = \frac{F_{(resonance)}}{2\Delta F}$$

where:

2ΔF is the difference between the frequencies, when the reactive component is equal to the resistive component at self-resonance at any bias voltage.

(The Q of the diode junction alone is the product of:

$$\text{the above } Q \times \frac{1}{1 + \frac{C_s}{C_o}}$$

where: C_s = stray capacitance
C_o = junction capacitance)

Note: The construction of a solid brass dummy diode for short-circuit reference will be necessary.

(b) The diode Q may be computed from the known junction capacitance and the VSWR at resonance in accordance with the following relationship:

$$Q = \frac{1}{2f_{(resonance)} \times \frac{10}{\Gamma} \times C_o} \times \frac{1}{1 + \frac{C_s}{C_o}}$$

where: Γ = VSWR normalized to 10 ohms in the test holder
C_s = stray capacitance
C_o = junction capacitance

4.8.3 Self-Resonance Frequency test.- The self-resonance frequency shall be determined from the test procedures per 4.8.2, Method A or B, herein.

4.8.4 Capacitance tests.- The specified voltage and a-c signal (see below) shall be applied to the terminals, and the capacitance shall then be measured. The junction capacitance C_o is the capacitance associated with the barrier at zero bias. Capacitance shall be measured at 100 Kc with a Boonton Electronics 74-C Capacitance Bridge, or equal. The a-c signal level applied to the junction shall be such that a 3 db increase in level produces less than a 10% change in junction capacitance. Junction capacitance may be calculated by subtracting the capacitance of the empty package from the measured total capacitance. The capacitance of the empty package, measured at 100 Kc, shall not exceed the limit specified (see Table I herein). The definition of "package" shall be: complete unit minus the gallium arsenide wafer.

4.8.5 Reverse Voltage Breakdown test. - The specified reverse current, and associated reverse bias voltage shall be applied to the terminals. Breakdown shall occur when the minimum specified reverse bias voltage level is reached.

4.8.6 Series Resistance test. - The measurement of series resistance shall be based upon the capacitance change of the diode, and shall be made at a frequency $\approx$ 10.0 kmc. The method of measurement shall be as mutually agreed upon between the contractor and the Contracting Officer or his authorized technical representative.

4.8.7 Normalized Incremental Capacitance test. - Determination of normalized incremental capacitance test shall be based upon a measurement of ΔC and C1 per the formula:

$$\text{Normalized Incremental Capacitance} = \frac{\Delta C}{C1}$$

Where: ΔC = difference between capacitance values at 2 voltage points at the extremes of the non-linear portion of the C-V curve.

C1 = measurement of the pump capacity at its terminals, when terminated by the diode.

The test procedure and test circuit(s) shall be as mutually agreed upon between the contractor and the Contracting Officer or his authorized technical representative.

4.8.8 Burnout test. - The specified d-c forward power, computed as the product of d-c forward current and d-c voltage drop, shall be applied to the diode for at least 10 seconds. The external temperature of the diode under test shall be at least 25° ± 3°C.

Table I. Group A inspection.

MIL-S-19500 Appx. C Ref. Par.	Examination or test	Conditions	LTPD	Max. Acc. No.	Symbol	Limits Min.	Limits Max.	Unit
	<u>Subgroup 1</u>		10	4				
30.13	Visual and mechanical inspection	---			---	---	---	---
	<u>Subgroup 2</u>		5	3				
1/	Frequency cutoff	V = -6Vdc			f_c	200	---	kmc
2/	Diode Q	---			Q	---	20	---
3/	Self-resonance frequency	---			f_r	10	---	kmc
	<u>Subgroup 3</u>		5	3				
4/	Junction capacitance	---			C_o	0.2	1.5	uuf
4/	Package capacitance	---			C_p	---	0.15	uuf
	<u>Subgroup 4</u>	I_r = 10μAdc	5	3				
5/	Reverse voltage breakdown				V_r	6.0	---	Vdc
6/	Series resistance	---			R_s	---	2.0	ohms
7/	Normalized incremental capacitance	---			$\frac{\Delta C}{CI}$	.4	---	uuf

1/ See 4.8.1
2/ See 4.8.2 herein.
3/ See 4.8.3 herein.
4/ See 4.8.4 herein.
5/ See 4.8.5 herein.
6/ See 4.8.6 herein.
7/ See 4.8.7 herein.

Table II. Group B Inspection.

MIL-S-19500 Appx. C R.F. Par.	Examination or test	Conditions	LTPD	Max. Acc. No.	Symbol	Limits Min.	Limits Max.	Unit
	Subgroup 1		20	3				
30.9	Physical dimensions	---			---	---	---	---
	Subgroup 2		20	3				
1/	Burnout	P = 500 mW			---	---	---	---
	End-point tests:							
2/	Frequency cutoff	V = -6Vdc			f_c	200	---	kmc
3/	Self-resonance frequency	---			f_r	1k	---	kmc
	Subgroup 3		1	4				
40.14	Temperature cycling	-195° to +200°C 4/			---	---	---	---
40.6	Moisture resistance	No initial conditioning			---	---	---	---
	End-point tests: Same as for Subgroup 2, above							
	Subgroup 4		20	[illegible]				
40.10	Shock	No voltage; G=500g 5 blows ea. of 1 msec ea. in orientations X1, Y1, Y2 (total blows = 15)			---	---	---	---

Table II. Group B Inspection - (Continued).

MIL-S-19500 Appx. C Ref. Par.	Examination or test	Conditions	LTPD	Max. Acc. No.	Symbol	Limits Min.	Limits Max.	Unit
	Subgroup 4 - (cont'd)							
40.20	Vibration, variable frequency	f = 50 to 2000 cps; 4 sweeps; 15G			---	---	---	---
40.4	Constant acceleration (centrifuge)	G = 20,000; Orientations X1, Y1, Y2			---	---	---	---
40.2	Axial strain	force = 1 lb.			---	---	---	---
	End-point tests: Same as for Subgroup 2, above							
	Subgroup 5							
40.7	Storage life	Method B T_A=200°C max t = 500 hrs.	λ = 10	---	---	---	---	---
	End-point tests: Same as for Subgroup 2, above							

1/ See 4.8.8 herein.

2/ See 4.8.1 herein.

3/ See 4.8.3 herein.

4/ Per Method 102A in Standard MIL-STD-202.

5. PREPARATION FOR DELIVERY

5.1 Preparation for delivery.- Preparation for delivery shall be in accordance with Specification MIL-S-19500.

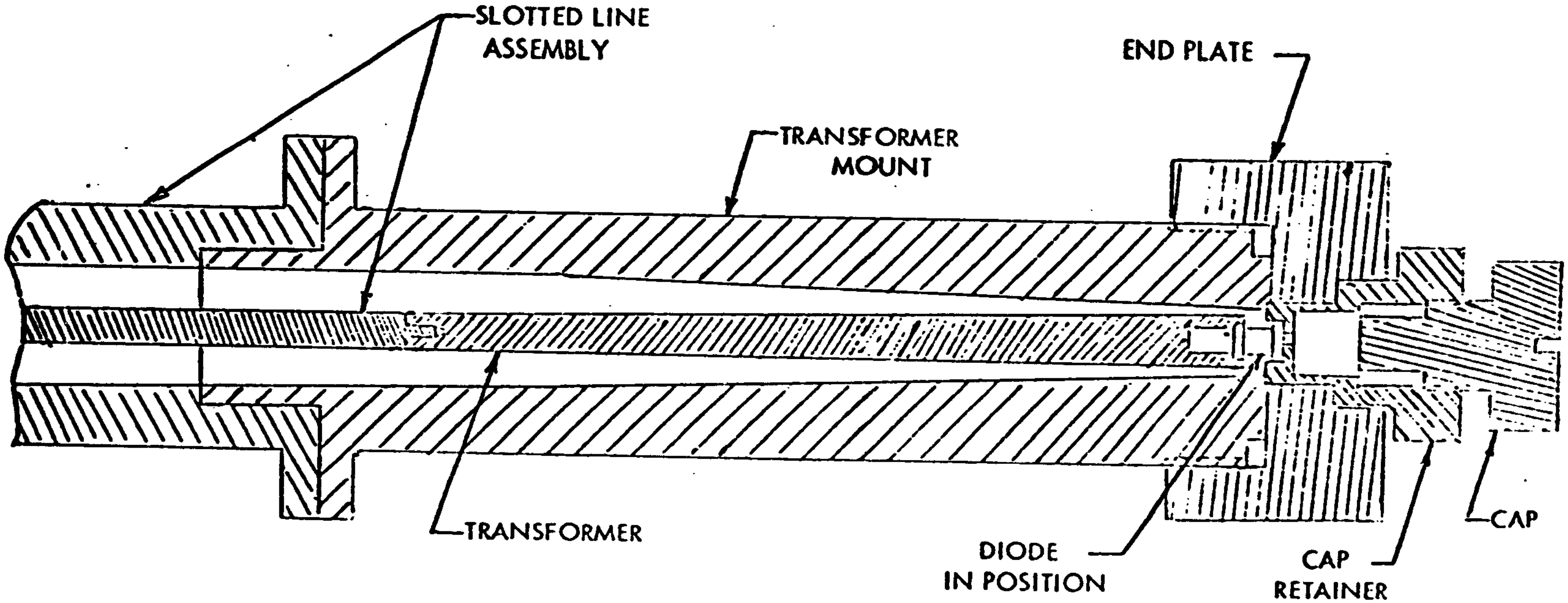
6. NOTES

6.1 Notes.- The notes included in Specification MIL-S-19500, except for those covering qualification (see 4.2 herein) and the following, are applicable to this document.

6.2 Ordering data.- If this document is used with the "C" or later issue of Specification MIL-S-19500 containing LTPD-method Acceptance Inspection requirements, the solicitation should indicate that the Acceptance Inspection LTPD-method requirements in paragraphs 4.3 through 4.3.3 herein shall be considered superseded by the pertinent requirements in the "C" or later issue of Specification MIL-S-19500.

6.3 Establishment of additional tests and parameters.- The resolution of any additional tests and parameters that will serve for optimum performance evaluation of the device relative to the application need is encouraged. It is expected that such determination(s) will be by mutual agreement between the contractor and the responsible Government agency, and will be included in the final acceptance criteria for the device. Pertinent electrical, physical, mechanical, and environmental test coverage in Specification MIL-S-19500 should be considered as a primary guide in this regard.

NOTICE: When Government drawings, specifications or other data are used for any purpose other than in connection with a definitely related Government procurement operation, the United States Government thereby incurs no responsibility nor any obligation whatsoever; and the fact that the Government may have formulated, furnished, or in any way supplied the said drawings, specifications, or other data is not to be regarded by implication or otherwise as in any manner licensing the holder or any other person or corporation, or conveying any right or permission to manufacture, use, or sell any patented invention that may in any way be related thereto.



NOTE: A drawing containing all requisite constructional and dimensional details for this test holder will be provided by the Contracting Officer.

Figure 1. Advance representation of diode test-holder.

Table III. Minimum size of sample to be tested to assure, with 90% confidence, an LTPD no greater than the LTPD specified.

Acceptance Number (c)	Maximum Percent Defective (LTPD) 1/								
	20	15	10	5	2	1	0.5	0.2	0.1
	Minimum Sample Sizes								
0	11 (0.46)	15 (0.34)	22 (0.23)	45 (0.11)	116 (0.04)	231 (0.02)	461 (0.01)	1152 (0.005)	2303 (0.002)
1	18 (2.0)	25 (1.4)	38 (0.94)	77 (0.46)	195 (0.18)	390 (0.09)	778 (0.045)	1946 (0.018)	3891 (0.009)
2	25 (3.4)	34 (2.24)	52 (1.6)	105 (0.78)	266 (0.31)	533 (0.15)	1065 (0.080)	2662 (0.031)	5323 (0.015)
3	32 (4.4)	43 (3.2)	65 (2.1)	132 (1.0)	333 (0.41)	668 (0.20)	1337 (0.10)	3341 (0.041)	6681 (0.018)
4	38 (5.3)	52 (3.9)	78 (2.6)	158 (1.3)	398 (0.50)	798 (0.25)	1599 (0.12)	3997 (0.049)	7994 (0.025)
5	45 (6.0)	60 (4.4)	91 (2.9)	184 (1.4)	462 (0.57)	927 (0.28)	1855 (0.14)	4638 (0.056)	9275 (0.028)
6	51 (6.6)	68 (4.9)	104 (3.2)	209 (1.6)	528 (0.62)	1054 (0.31)	2107 (0.155)	5267 (0.062)	10,533 (0.031)
7	57 (7.2)	77 (5.3)	116 (3.5)	234 (1.7)	589 (0.67)	1178 (0.34)	2355 (0.17)	5886 (0.067)	11,771 (0.034)
8	63 (7.7)	85 (5.6)	128 (3.7)	258 (1.8)	648 (0.72)	1300 (0.36)	2599 (0.18)	6498 (0.072)	12,995 (0.036)
9	69 (8.1)	93 (6.0)	140 (3.9)	282 (1.9)	709 (0.77)	1421 (0.39)	2842 (0.19)	7103 (0.077)	14,206 (0.039)
10	75 (8.4)	100 (6.3)	152 (4.1)	306 (2.0)	770 (0.80)	1541 (0.40)	3032 (0.20)	7704 (0.08)	15,407 (0.04)
(r = c + 1)	1/ The minimum quality (approximate AQL percent defective) required to accept (on the average) 19 to 20 lots is indicated in parentheses, respectively below, for information purposes only.								

APPENDIX B

Data for Engineering Samples

submitted this Quarter

SYLVANIA ELECTRIC PRODUCTS INC.

SEMI-CONDUCTOR DIVISION

Sheet No. 1 of III

Test Dept. ______

Type ______

Lot No. ______

Proj. No. ______

Test Oper. ______

Engineer ______

Date 30 January 1963

Job No. ______

Nature of Test

☐ Electrical

☐ Environmental

☐ Storage ☐ 25°C ☐ 85°C ☐ __°C Hours ______

☐ Temp. Cycle ___°C ___°C ___°C

☐ Moisture Resis.

☐ Mechanical

☐ Centrifuge ____ G's

☐ Vibration ____ ~ ____ G's ____ G's

☐ Shock ____ G's

Remarks Data for Second Group 75 Engineering Samples Gallium Arsenide Varactor Diode

Contract No. DA-36-039-SC-86736

Order No. 19058-PP-62-81-81

Background: Requested by ______ Dept. ______ Date Recd. ______ ☐ Prod. ☐ Devel. ☐ Comp.

Cond. / Spec. / Unit	B.V	C_p	C_J	F_{co}	Q	R_s
	10 μa	μμf	0 v.	-6 v.	-6 v	ohms
1	7.5	.35	.439	111.0	11.7	8.8
2	9.0	.35	.447	116.0	12.3	8.6
3	6.2	.35	.360	103.0	10.9	12.0
4	16.4	.35	.365	57.8	6.1	19.0
5	6.0	.35	.343	86.8	9.1	17.5
6	8.0	.35	.517	109.0	11.5	6.9
7	7.2	.35	.278	76.0	8.0	17.5
8	8.0	.35	.433	137.0	14.4	7.0
9	9.0	.35	.439	103.0	10.9	8.5
10	5.6	.35	.422	81.2	8.5	11.5
11	6.8	.35	.339	91.2	8.5	13.5
12	6.6	.35	.405	96.0	10.1	10.0
13	9.5	.35	.341	85.2	9.1	13.0
14	8.4	.35	.445	97.5	10.3	9.1
15	7.0	.35	.349	76.0	8.0	14.0
16	8.8	.35	.419	75.2	7.9	13.0
17	8.0	.35	.538	91.0	9.6	8.6
18	9.2	.35	.509	99.0	9.9	8.2
19	8.4	.35	.700	105.0	11.1	5.5
20	9.0	.35	.101	70.0	7.4	53.0
21	15.0	.35	.109	77.2	8.1	32.0
22	17.0	.35	.057	70.8	7.5	50.0
23	12.0	.35	.255	78.4	8.3	18.0
24	5.2	.35	.213	92.0	9.7	20.0
25	9.2	.35	.207	123.0	13.0	15.0

SYLVANIA ELECTRIC PRODUCTS INC.

SEMI-CONDUCTOR DIVISION

Sheet No. II of III
Test Dept. ______
Type ______
Lot No. ______
Proj. No. ______
Test Oper. ______
Engineer ______
Date 30 January 196
Job No. ______

Nature of Test

☐ Electrical

☐ Environmental
☐ Storage
☐ 25°C ☐ 85°C ☐ ___°C
Hours ______
☐ Temp. Cycle
___°C ___°C ___°C
☐ Moisture Resis.

☐ Mechanical
☐ Centrifuge ______ G's
☐ Vibration ______ ~
______ G's ______ G's
☐ Shock ______ G's

Remarks Data for Second Group 75 Engineering Samples Gallium Arsenide Varactor Diode
Contract No. DA-36-039-SC-86736
Order No. 19058-PP-62-81-81

Background: Requested by ______ Dept. ______ Date Recvd. ______ ☐ Prod. ☐ Devel. ☐ Comp.

Cond.	B.V.	C_p	C_r	F_{co}	Q-6	R_s
Spec. / Unit	10μa	μμf.	0 bias	-6 bias	-6 bias	ohms
26	5.3	.350	.376	99	10.4	11.0
27	9.3	.350	.318	126	13.3	11.0
28	15.8	.350	.196	81.2	8.5	24.0
29	8.7	.350	.720	70.0	7.4	.7.9
30	9.7	.350	.109	67.0	7.2	50.0
31	10.8	.350	.139	73.0	7.8	25.0
32	9.6	.350	.142	76.0	8.0	38.0
33	7.7	.350	.161	80.0	8.4	32.0
34	16.6	.350	.542	103.0	10.9	7.0
35	10.8	.350	.192	83.0	8.8	25.0
36	14.4	.350	.153	91.0	9.6	29.0
37	15.6	.350	.232	92.0	9.7	13.0
38	7.4	.350	.435	88.0	9.3	10.0
39	12.0	.350	.820	90.0	9.5	5.2
40	8.2	.350	.206	82.0	8.6	18.0
41	11.0	.350	.515	92.0	9.7	9.0
42	8.0	.350	.623	89.0	9.3	9.0
43	10.0	.350	.497	80.0	8.5	12.0
44	8.4	.350	.410	73.6	7.8	12.5
45	8.8	.350	.168	67.6	7.8	40.0
46	5.8	.350	.807	70.0	7.4	26.0
47	15.3	.350	.930	64.0	6.8	6.0
48	9.6	.350	.355	64.0	6.8	19.0
49	10.7	.350	.887	64.0	6.8	6.5
50	15.8	.350	.311	57.0	6.1	23.0

SYLVANIA ELECTRIC PRODUCTS INC.

SEMI-CONDUCTOR DIVISION

Sheet No. III of III

Test Dept. ______

Type ______

Lot No. ______

Proj. No. ______

Test Oper. ______

Engineer ______

Date 30 January 1963

Job No. ______

Nature of Test

☐ Electrical

☐ Environmental

☐ Storage
☐ 25°C ☐ 85°C ☐ ___°C
Hours ______

☐ Temp. Cycle
___°C ___°C ___°C

☐ Moisture Resis.

☐ Mechanical

☐ Centrifuge ______ G's

☐ Vibration ______ ~
______ G's ______ G's

☐ Shock ______ G's

Remarks Data for Second Group 75 Engineering Samples Gallium Arsenide Varactor Diode

Contract No. DA-36-039-SC-86736

Order No. 19058-PP-62-81-81

Background: Requested by ______ Dept. ______ Date Recvd. ______ ☐ Prod. ☐ Devel. ☐ Comp.

Cond. / Spec. / Unit	B.V	C_p	C_J	F_{co}	Q	R_s
	10 μa	μμf	0 v.	-6 v.	-6 V	ohms
51	9.3	.35	.473	66.0	7.0	13.5
52	7.0	.35	1.280	64.0	6.8	55.0
53	15.4	.35	.690	60.2	6.4	11.0
54	15.6	.35	.167	62.0	6.6	40.0
55	18.9	.35	.173	64.0	6.8	30.0
56	9.0	.35	.087	66.8	7.1	50.0
57	6.2	.35	.541	77.0	8.1	8.5
58	7.2	.35	.408	74.0	7.8	11.0
59	9.0	.35	.424	98.0	10.3	9.0
60	7.5	.35	.690	101.0	10.6	6.0
61	6.5	.35	.237	66.8	7.1	27.0
62	7.0	.35	.280	82.0	8.6	17.0
63	6.0	.35	.414	91.0	9.6	9.0
64	7.0	.35	.780	84.0	8.8	6.0
65	6.5	.35	.930	66.0	6.9	7.0
66	7.8	.22	.145	99.0	10.4	32.0
67	6.6	.22	.406	85.2	8.9	13.0
68	9.2	.22	.295	116.0	12.2	12.0
69	8.4	.22	.320	82.0	8.6	16.0
70	7.2	.22	.159	90.0	9.5	38.0
71	6.0	.22	.385	114.0	12.0	8.1
72	9.4	.22	.088	78.4	8.3	6.8
73	9.2	.22	.341	126.0	13.3	8.3
74	8.2	.22	.630	111.0	11.1	7.1
75	6.6	.22	.233	78.4	8.3	24.0

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